

## CLAIMS

1. A method of performing Viterbi decoding function comprising the steps of:

calculating candidate path metrics for states at time  $T_n$  based on previously calculated path metrics for states at time  $T_{n-1}$  and branch metrics associated with transitions between said states at time  $T_{n-1}$  and states at time  $T_n$  according to a first trellis;

selecting path metrics for states at time  $T_n$  from said candidate path metrics;

calculating candidate path metrics for states at  $T_{n+1}$  based on said selected path metrics for states at  $T_n$  according to a second trellis, different from said first trellis.

2. The method of claim 1 wherein said step of calculating candidate path metrics according to a first trellis comprises the step of simultaneously calculating path metrics for a group of states at  $T_n$ .

3. The method of claim 2 and further comprising the step of repeating said step of calculating path metrics for a group of states at  $T_n$  until path metric candidates for all states at  $T_n$  are generated.

4. The method of claim 2 wherein said step of simultaneously calculating path metrics for a group comprises the steps of:

for each of  $j$  sets of states at  $T_{n-1}$ , loading fields associated with a first operand of a processing device with respective path metrics of the set, loading a second operand of said processing device with corresponding branch metrics, adding said first and second operands to generate a result providing candidate path metrics for said group of states at  $T_n$  in respective fields of the result.

5. The method of claim 4 and further comprising the step of storing  
the result for each of said  $j$  sets in respective registers.

6. The method of claim 5 wherein said selecting step comprises the  
step of comparing respective fields of said registers to determine a smallest path  
metric for each state of said group.

7. The method of claim 6 and further comprising the step of updating  
a traceback array.

8. The method of claim 1 wherein said step of calculating candidate  
path metrics according to a second trellis comprises the step of simultaneously  
calculating path metrics for a group of states at  $T_{n+1}$ .

9. The method of claim 8 and further comprising the step of repeating  
said step of calculating path metrics for a group of states at  $T_n$  until path metric  
candidates for all states at  $T_{n+1}$  are generated.

10. The method of claim 8 wherein said step of simultaneously  
calculating path metrics for a group of states at  $T_{n+1}$  comprises the steps of:  
loading fields associated with a first operand of a processing device with  
respective path metrics of a set of states at  $T_n$ , loading respective fields of a  
second operand of said processing device with corresponding branch metrics,  
adding said first and second operands to generate a result providing candidate  
path metrics for said group of states at  $T_{n+1}$  in respective fields of the result.

11. The method of claim 10 and further comprising the step of  
generating additional candidate path metrics for said group of states at  $T_{n+1}$  by  
rotating the fields in said first operand, loading respective fields of the second  
operand with corresponding state metrics and adding said first and second  
operands.

12. A Viterbi decoder comprising:

programmable processing circuitry for:

calculating candidate path metrics for states at time  $T_n$  based on

previously calculated path metrics for states at time  $T_{n-1}$  and branch metrics associated with transitions between said states at time  $T_{n-1}$  and states at time  $T_n$

according to a first trellis;

selecting path metrics for states at time  $T_n$  from said candidate path

metrics;

calculating candidate path metrics for states at  $T_{n+1}$  based on said

selected path metrics for states at  $T_n$  according to a second trellis, different from said first trellis.

13. The Viterbi decoder of claim 12 wherein said programmable

processing circuitry calculates candidate path metrics according to a first trellis by simultaneously calculating path metrics for a group of states at  $T_n$ .

14. The Viterbi decoder of claim 13 wherein said programmable

processing circuitry repeats the calculation of path metrics for a group of states at  $T_n$  until path metric candidates for all states at  $T_n$  are generated.

15. The Viterbi decoder of claim 13 wherein said programmable

processing circuitry includes a arithmetic unit operable to perform multiple simultaneous logic operations on respective fields of first and second operands.

16. The Viterbi decoder of claim 15 wherein path metrics for a group

are calculated by:

for each of  $j$  sets of states at  $T_{n-1}$ , loading fields associated with the first

operand with respective path metrics of the set, loading the second operand of with corresponding branch metrics, adding said first and second operands to

6 generate a result providing candidate path metrics for said group of states at  $T_n$   
in respective fields of the result.

17. The Viterbi decoder of claim 16 wherein said programmable  
2 processing circuitry includes respective registers for storing the result for each of  
said  $j$  sets.

18. The Viterbi decoder of claim 17 wherein programmable processing  
2 circuitry selects path metrics by comparing respective fields of said registers to  
determine a smallest path metric for each state of said group.

19. The Viterbi decoder of claim 18 wherein said programmable  
2 processing circuitry stores said smallest path metrics in a traceback array.

20. The Viterbi decoder of claim 12 wherein said programmable  
2 processing circuitry calculates candidate path metrics according to a second  
trellis by simultaneously calculating path metrics for a group of states at  $T_{n+1}$ .

21. The Viterbi decoder of claim 20 wherein said programmable  
2 processing circuitry repeats calculating path metrics for a group of states at  $T_n$   
until path metric candidates for all states at  $T_{n+1}$  are generated.

22. The Viterbi decoder of claim 21 wherein said programmable  
2 processing circuitry includes an arithmetic unit operable to perform multiple  
simultaneous logic operations on respective fields of first and second operands.

23. The Viterbi decoder of claim 20 wherein said programmable  
2 processing circuitry calculates path metrics for a group of states at  $T_{n+1}$  by  
loading fields associated with the first operand of a processing device with  
4 respective path metrics of a set of states at  $T_n$ , loading respective fields of the  
second operand of said processing device with corresponding branch metrics,  
6 and adding said first and second operands to generate a result providing

candidate path metrics for said group of states at  $T_{n+1}$  in respective fields of the  
8 result.

24. The Viterbi decoder of claim 23 wherein said programmable  
2 processing device generates additional candidate path metrics for said group of  
states at  $T_{n+1}$  by rotating the fields in said first operand, loading respective fields  
4 of the second operand with corresponding state metrics and adding said first and  
second operands.